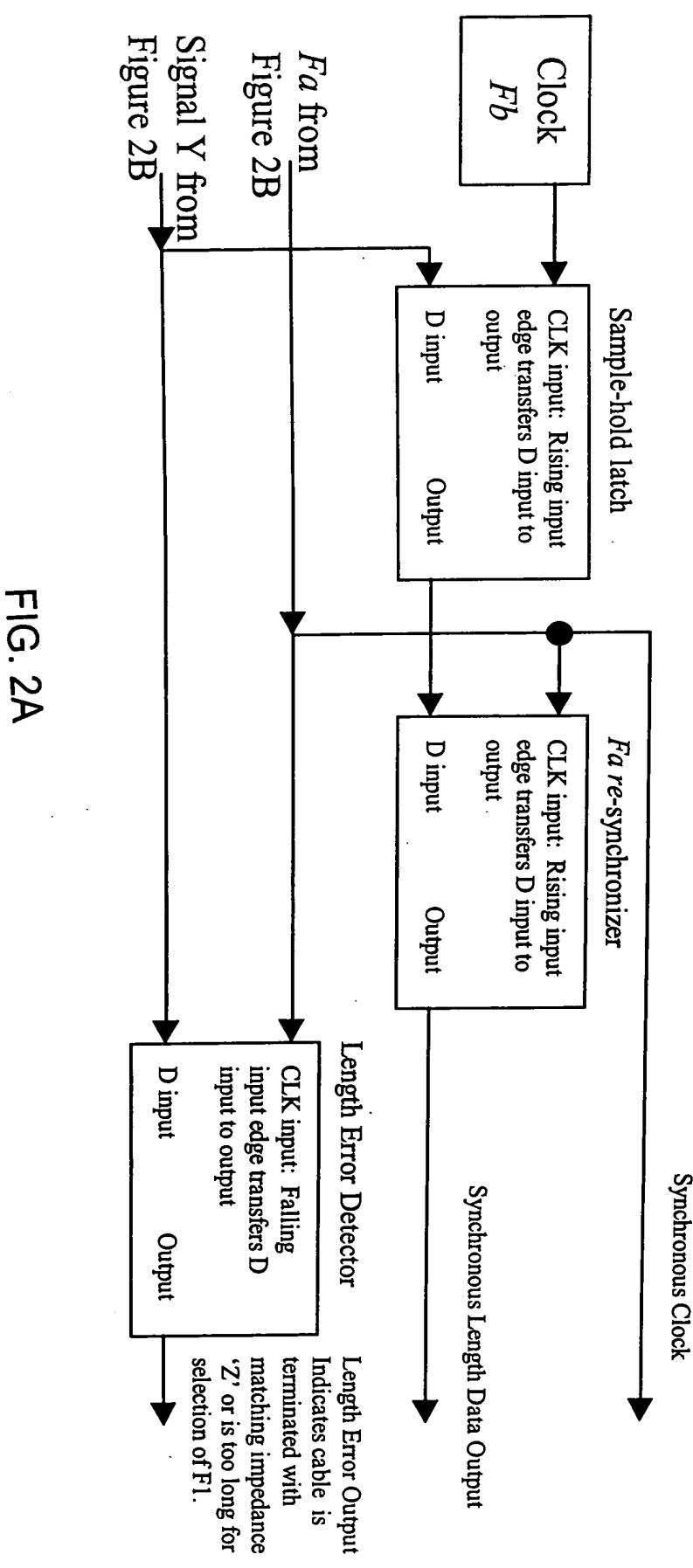


FIG. 1

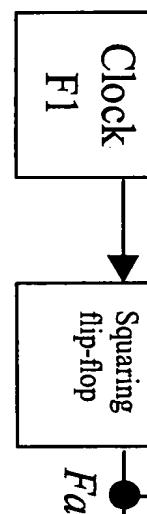
# PULSE WIDTH TESTING AND DATA OUTPUT SECTION



**CABLE-LENGTH-CONTROLLED  
PULSE WIDTH OSCILLATOR SECTION**

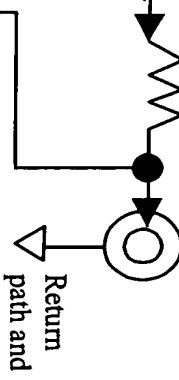
*F<sub>a</sub>* to Figure 2A  
*Signal Y* to Figure 2A

Connector to  
cable under  
test and  
impedance Z



*Clear Q to 0 when low*

Line Driving Amp  
*V<sub>+</sub>*  
*R*=*Z<sub>C</sub>*



Return path and  
GND

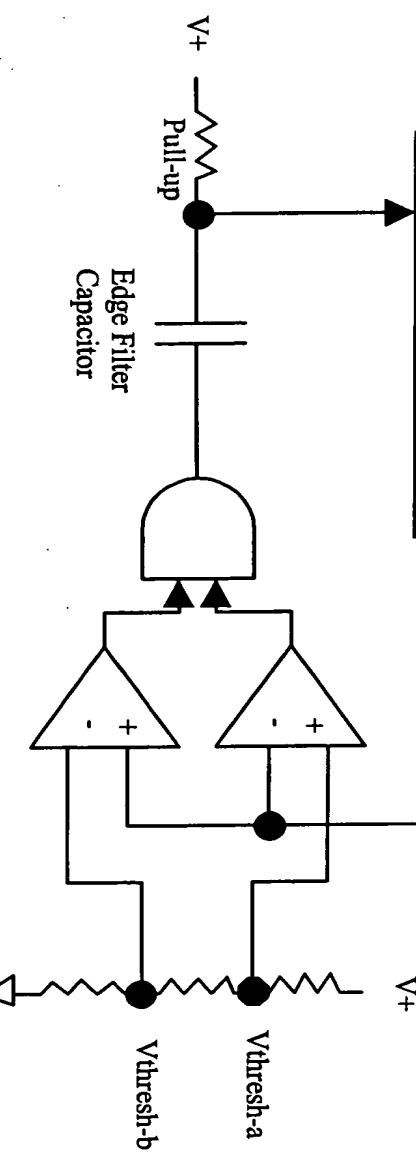
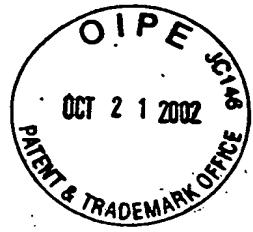


FIG. 2B

Combined Voltage Comparators



**Divide by N1**

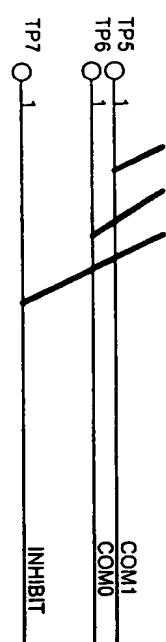
**F1 & F3**

**Generator**

(See Addendum)

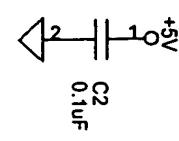
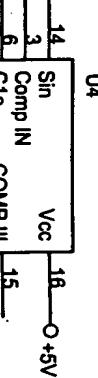
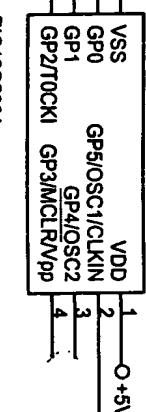


Not Used in this Article



**Divide by N1**

(See Addendum)

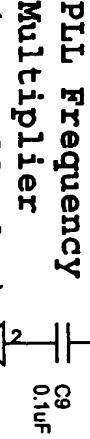


R1

R2

**PLL Frequency Multiplier**

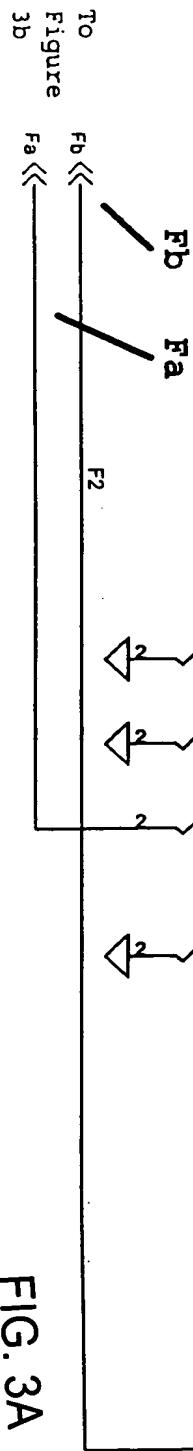
(See Addendum)



+5V  
0.1uF

C9

12  
1  
R5  
10K  
C7  
0.1uF



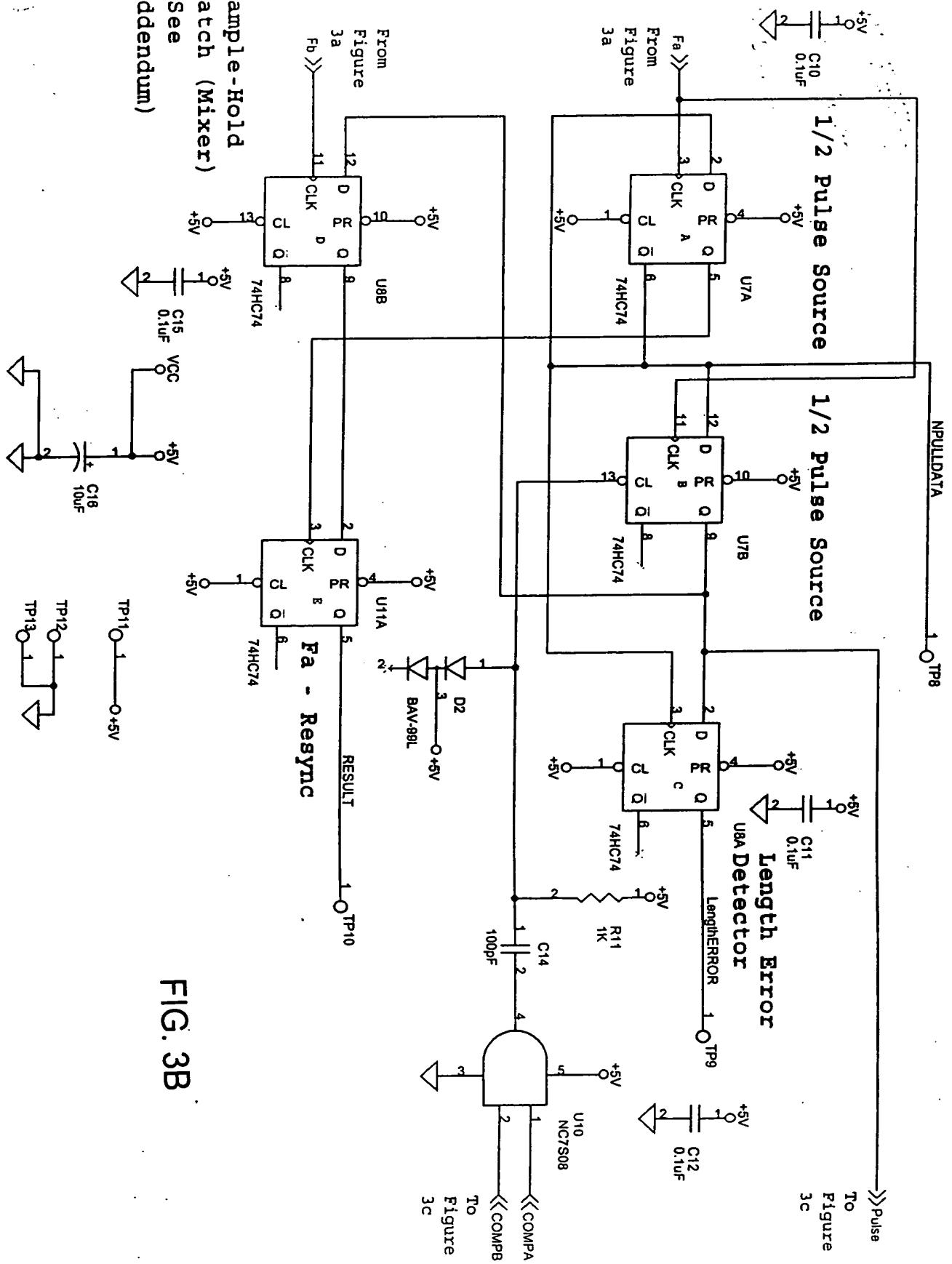
**FIG. 3A**

To Figure 3b

Fb <<

Fa <<







From  
Figure  
3b

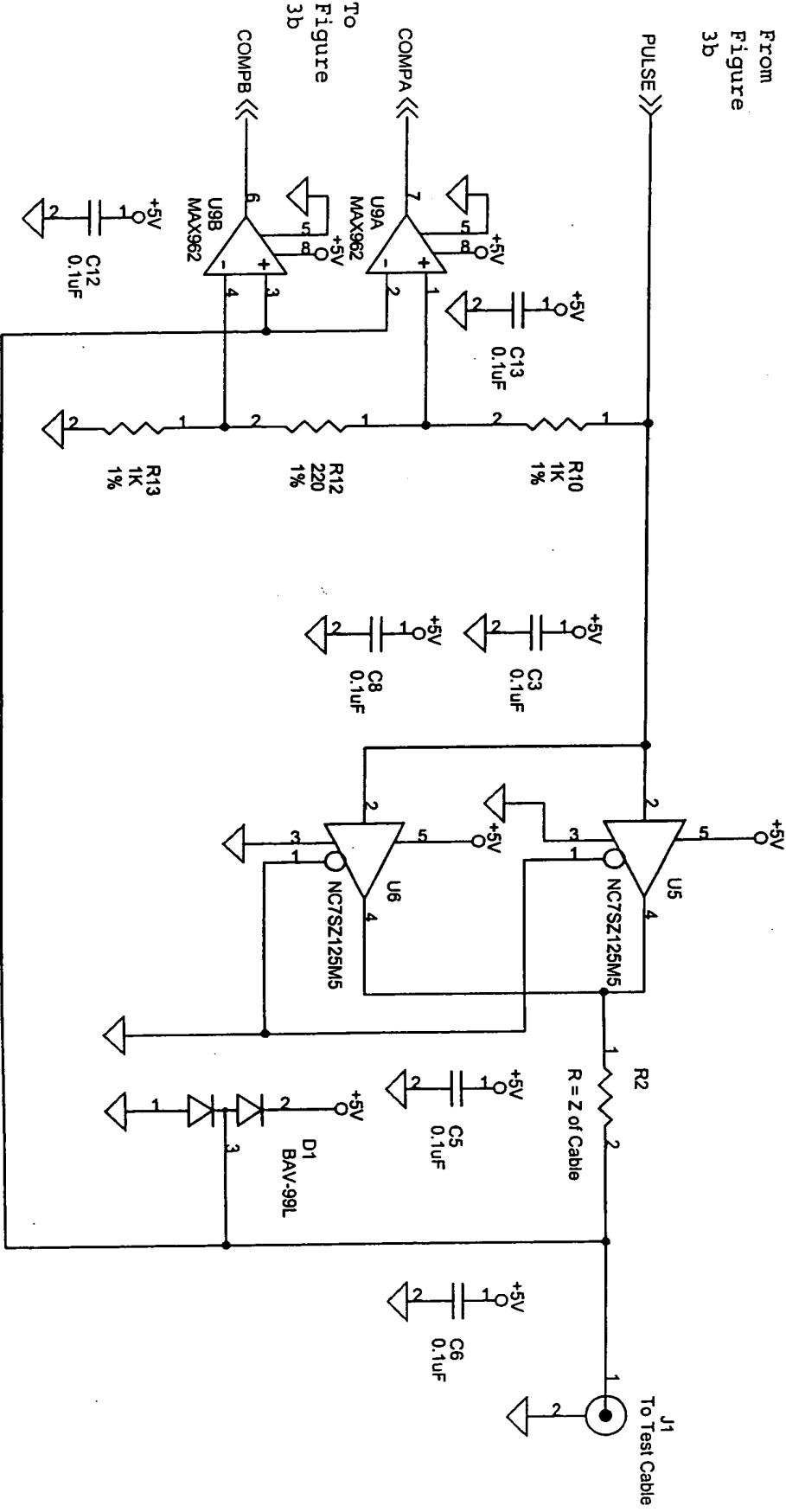
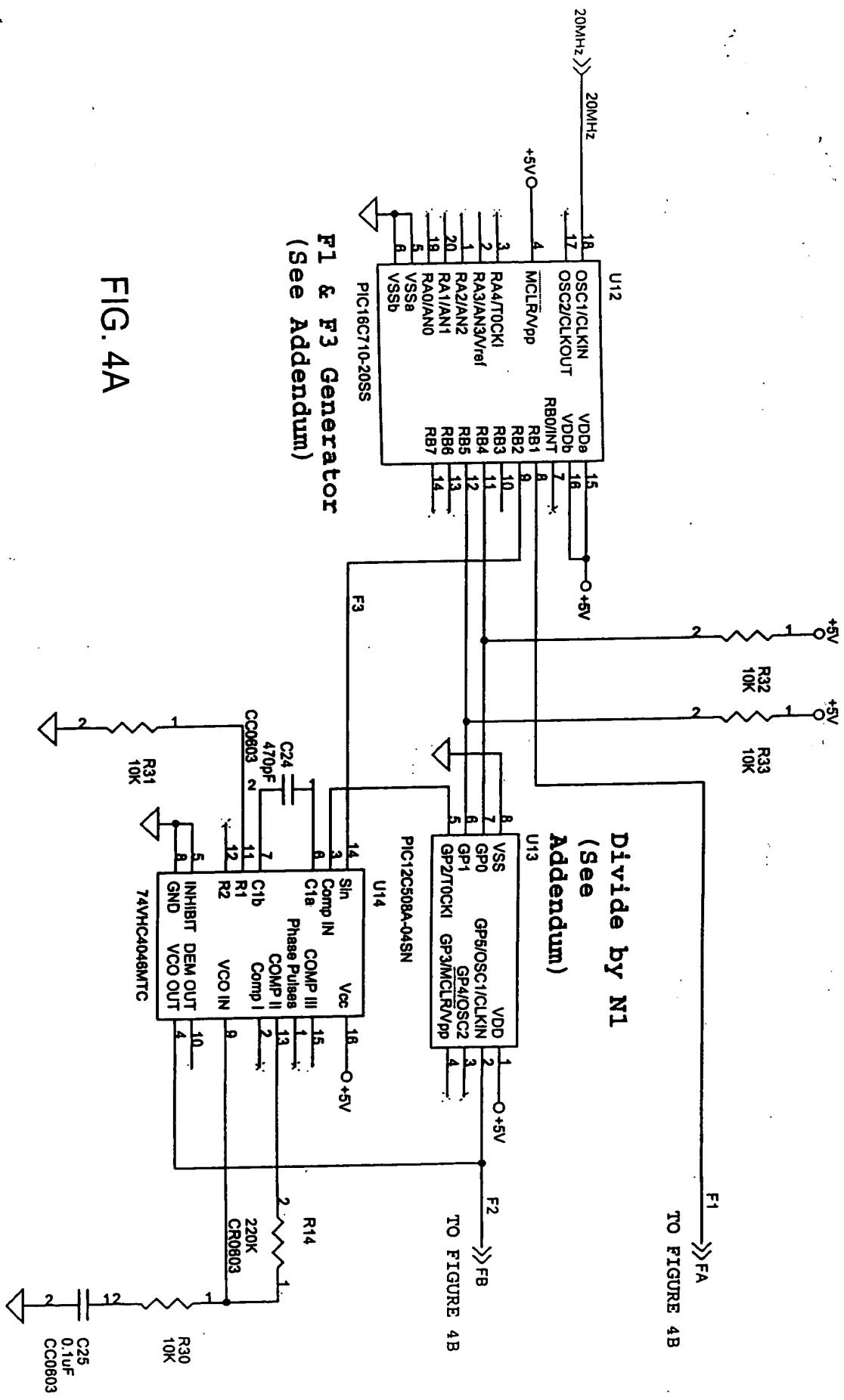
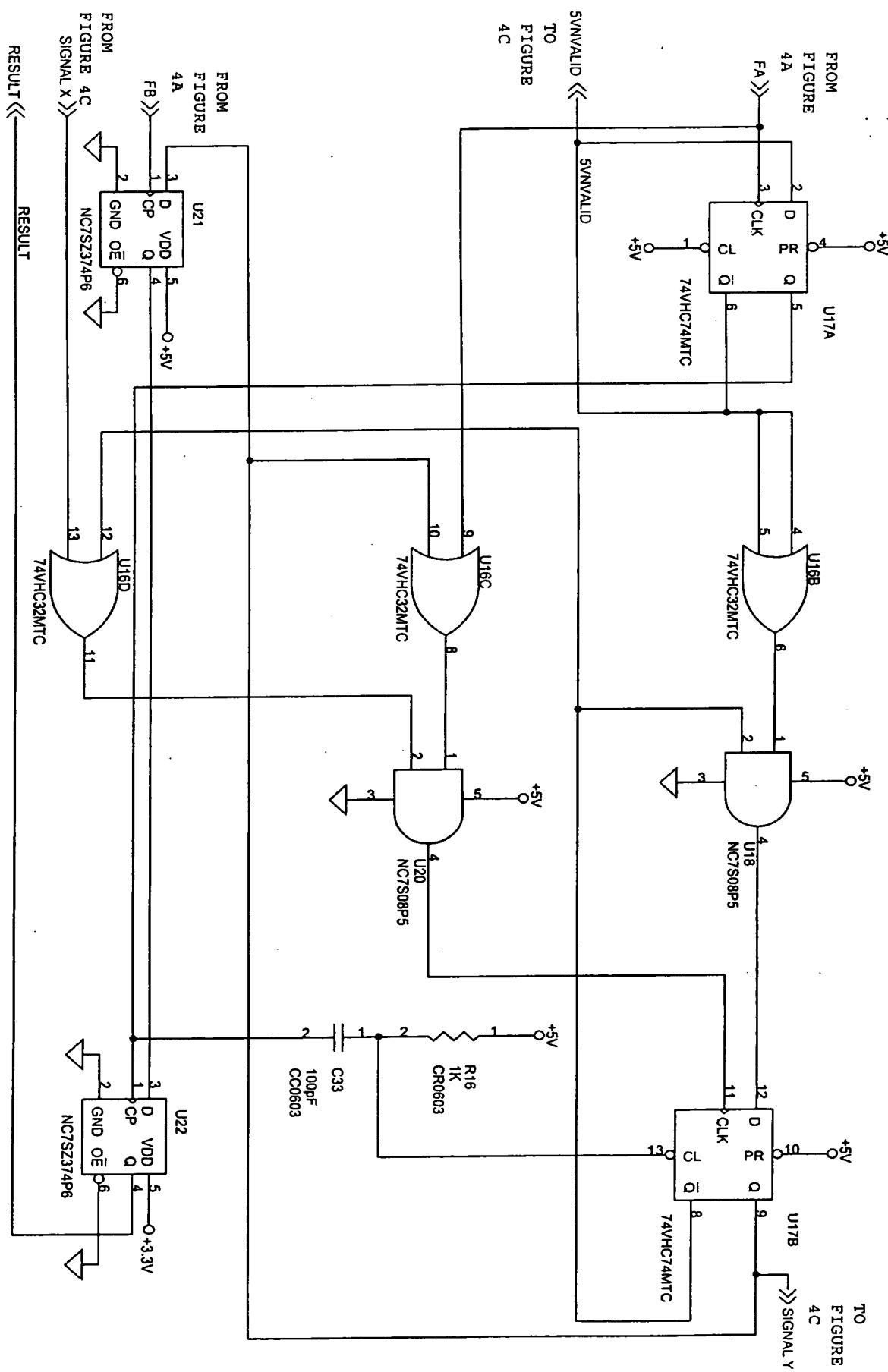
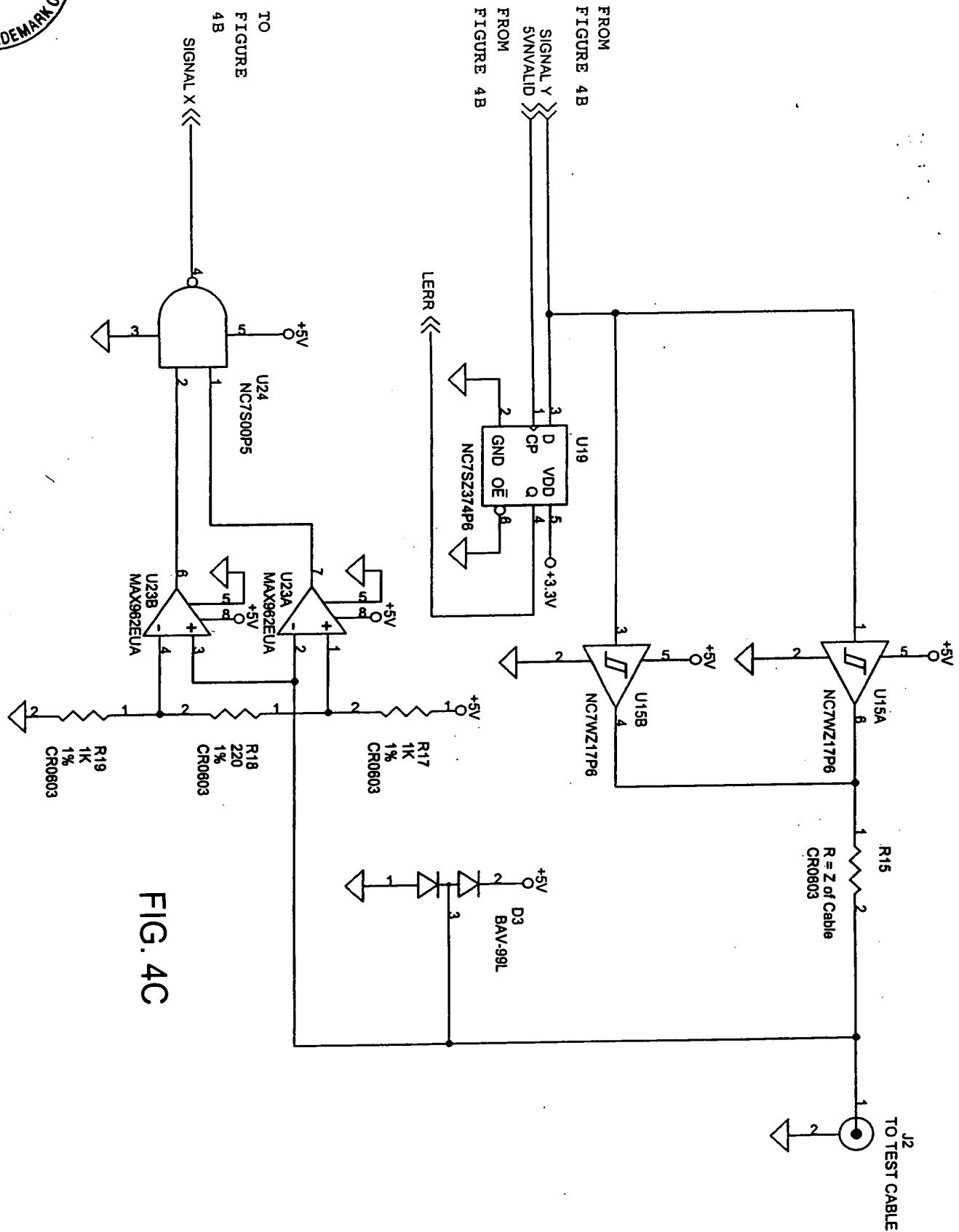
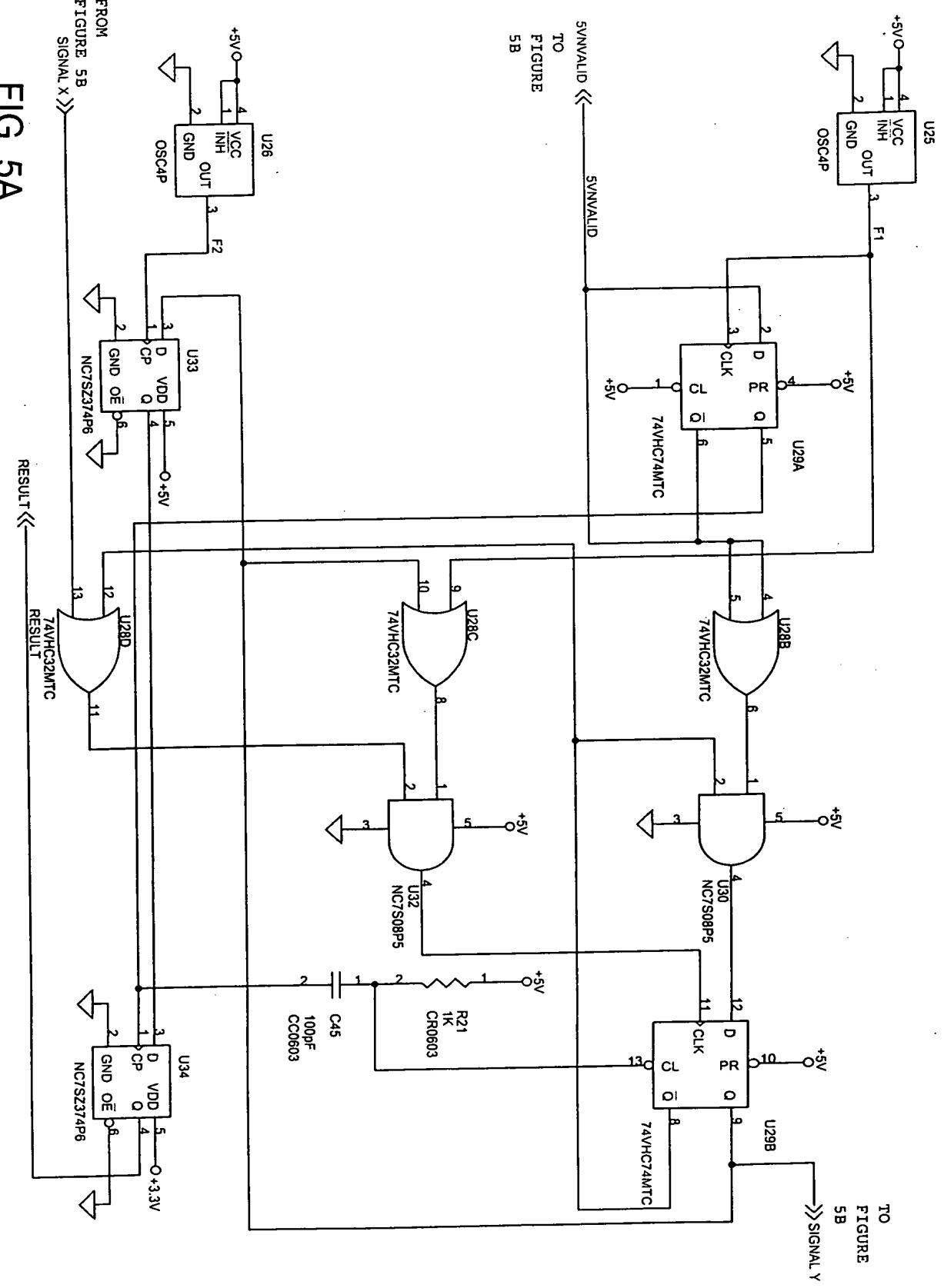


FIG. 3C











FROM FIGURE 5A

5V/VALIB

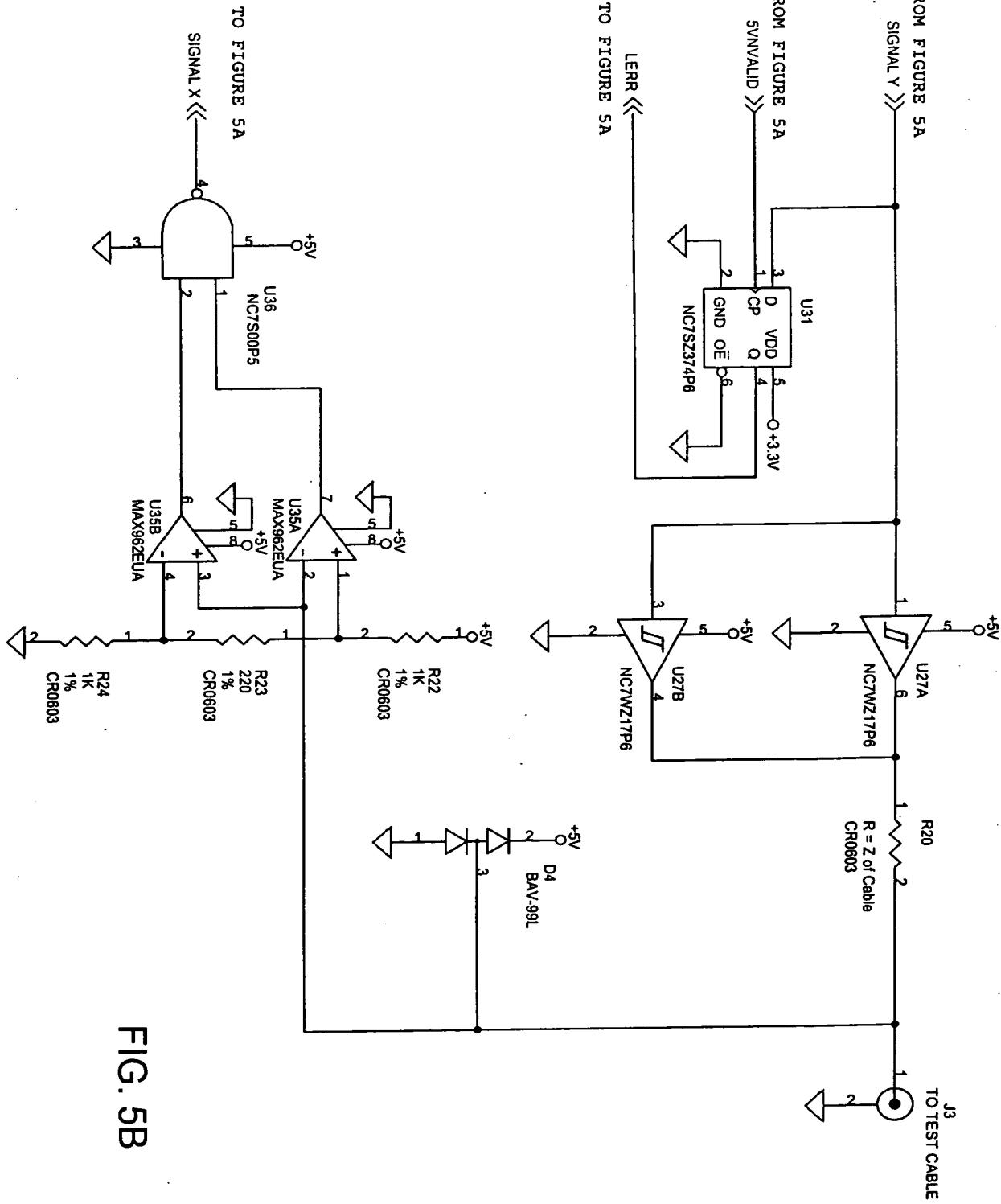




FIG. 6A

